Energy Conversion
Circuit Laboratory

Compact Drive Circuit for Capacitive Wireless Power Transfer System Utilizing Leakage-Enhanced Transformer

Hee-Su Choi & Sung-Jin Choi

Journal of Electrical Engineering & Technology

ISSN 1975-0102

J. Electr. Eng. Technol.
DOI 10.1007/s42835-018-00005-9

Springer

Energy Conversion
Circuit Laboratory

Your article is protected by copyright and all rights are held exclusively by The Korean Institute of Electrical Engineers. This e-offprint is for personal use only and shall not be self-archived in electronic repositories. If you wish to self-archive your article, please use the accepted manuscript version for posting on your own website. You may further deposit the accepted manuscript version in any repository, provided it is only made publicly available 12 months after official publication or later and provided acknowledgement is given to the original source of publication and a link is inserted to the published article on Springer's website. The link must be accompanied by the following text: "The final publication is available at link.springer.com".

Springer

Author's personal copy

Energy Conversion
Journal of Electrical Engineering & Technology
https://doi.org/10.1007/s42835-018-00005-9

ORIGINAL ARTICLE

Compact Drive Circuit for Capacitive Wireless Power Transfer System Utilizing Leakage-Enhanced Transformer

Hee-Su Choi[1] · **Sung-Jin Choi**[2]

Received: 13 May 2018 / Revised: 13 July 2018 / Accepted: 11 November 2018
© The Korean Institute of Electrical Engineers 2019

Abstract
In capacitively-coupled wireless power transmission (C-WPT), drive circuit topologies with various impedance matching or compensation techniques have been widely investigated in conventional studies, but they tend to increase the circuit complexity and thus offset the simplicity of the energy link structure which is a unique advantage over the inductively-coupled power transmission. In this paper, through systematic considerations on various matching schemes, a compact drive circuit with leakage-enhanced transformer is proposed in order to minimize the circuit volume for the capacitive power transfer system. In the proposed topology, the integrated transformer handles quality factor control as well as reactive compensation. Consequently, it reduces the number of components, the overall system volume, and the voltage stress of the energy link capacitor. The optimal design guideline of the leakage-enhanced transformer is also presented. Comparisons with the conventional method considering the circuit volume and component stress show the advantage of the proposed scheme, and feasibility of the new topology is verified with 10 W prototype hardware.

Keywords Impedance matching · Wireless power transfer · Magnetic integration · Volume reduction

1 Introduction

Nowadays, wireless power transfer is providing improved user experience in battery-operated systems due to its charging convenience and waterproof function [1–5]. While inductively-coupled power transmission (I-WPT) adopts a complex coil structure, capacitively-coupled wireless power transmission (C-WPT) utilizes link capacitors composed of pairs of conductors as shown in Fig. 1. The energy link structure is thus simplified, and the system cost can be further reduced by removing the coils.

In C-WPT systems, since the capacitance obtainable from the energy link structure is usually very small and its high reactance hinders the power flow, impedance matching is essential for reactance compensation and has been proposed in many studies. The simplest method of compensation is to connect series inductance such as a series resonant network [6] or an LCL compensator [7]. In this case, a large inductance value is needed because the series inductor compensates for the small capacitive reactance, and the quality factor of the resonant network becomes large, rendering the output voltage gain curve too narrow and sharp, while the voltage stress in the link capacitor increases considerably. Solve these problems LCLC compensation can address these drawbacks, but has eight components that need to be added [8].

Table 1 shows a summary of three recently announced topologies with a reasonable number of circuit components: LLC [9], double-side LC [10], and CLC [11] compensation networks. In the table, the input matching network (IMN) and the output matching network (OMN) denote the matching circuits in the transmitter and in the receiver, respectively. In the case of the LLC compensation [9], a 4.2 W was demonstrated with 6.78 MHz high frequency operation using two separate inductors located in the transmitter and the receiver side. Double-sided LC compensation [10] was used in the 150 W system to mitigate the low link capacitance problem. The CLC compensation structure in [11] is a topology that focuses on reducing the voltage

✉ Sung-Jin Choi
sjchoi@ulsan.ac.kr

Hee-Su Choi
sky911020@naver.com

[1] Silicon Mitus, Inc., Seongnam, South Korea

[2] School of Electrical Engineering, University of Ulsan, Ulsan, South Korea

Published online: 03 January 2019

Author's personal copy

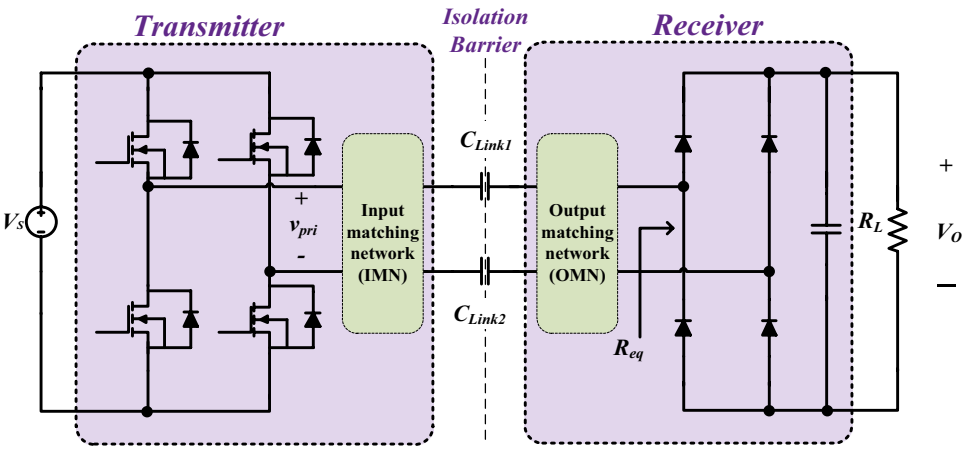


Fig. 1 Basic structure of C-WPT

Table 1 Conventional impedance matching methods

Refs.	IMN	OMN
[9]	L_1	L_2
[10]	L_1, C_1	L_2, C_2
[11]	C_1, L_2, L_1	C_2, L_3

stress in the link capacitors in a 1 KW capacitively-coupled wireless power system. While advantages for conventional topologies shown in Table 1 have been claimed individually, no studies have been conducted on the allocation of the matching network in view of the system volume reduction.

The purpose of this paper is to develop an effective matching topology that further simplifies the matching network structure in the C-WPT system. By introducing a transformer-based matching technique in a well-designed location, the proposed circuit minimizes the number of components required and reduces the volume of the matching network, which further strengthens the merits of the C-WPT technology. It should be noted that this topology mainly focuses on small or medium power applications with the output power of less than hundreds of watts such as consumer and portable electronic products that strictly require system volume reduction.

This paper consists of six sections. Section 2 discusses how an effective location for the matching structure is obtained by shifting its position in the series resonant structure. Section 3 explains the concept and operation principle of a leakage-enhanced transformer and presents the optimum design procedure. Section 4 compares the proposed matching circuit with the conventional matching circuit shown in Table 1 in terms of volume, loss, and voltage stress. Finally, in Sect. 5, the 50 W prototype hardware is tested for verification, and a conclusion is drawn in Sect. 4.

2 Consideration of Optimum Location of Impedance Matching

In view of the simplicity of the matching networks, magnetic transformers are an effective solution because they provide multiple functions such as impedance transformation or voltage gain modification, and they can be easily integrated with another neighboring inductive component. In order to find the optimal transformer matching locations, three schemes were compared as shown in Fig. 2 (a) series inductor matching, (b) input transformer matching with series inductor, and (c) output transformer matching with series inductor. The transformer used for the matching is regarded as an ideal component that has no leakage and no magnetizing inductance, and its turn ratio (N) is larger than unity (Fig. 3).

Generally, it is very important to design the moderate quality factor in the resonant tank because it determines the voltage stress in the energy link structure of the C-WPT system affecting the electrode design and safety. Also, it is known that the voltage stress of the link capacitor increases in proportion to the quality factor of the resonant network, as shown in (1).

$$V_{C,stress} = V_{pri}Q. \tag{1}$$

In the series inductor compensation scheme shown in Fig. 2a, a large inductance value is needed because the series

Author's personal copy

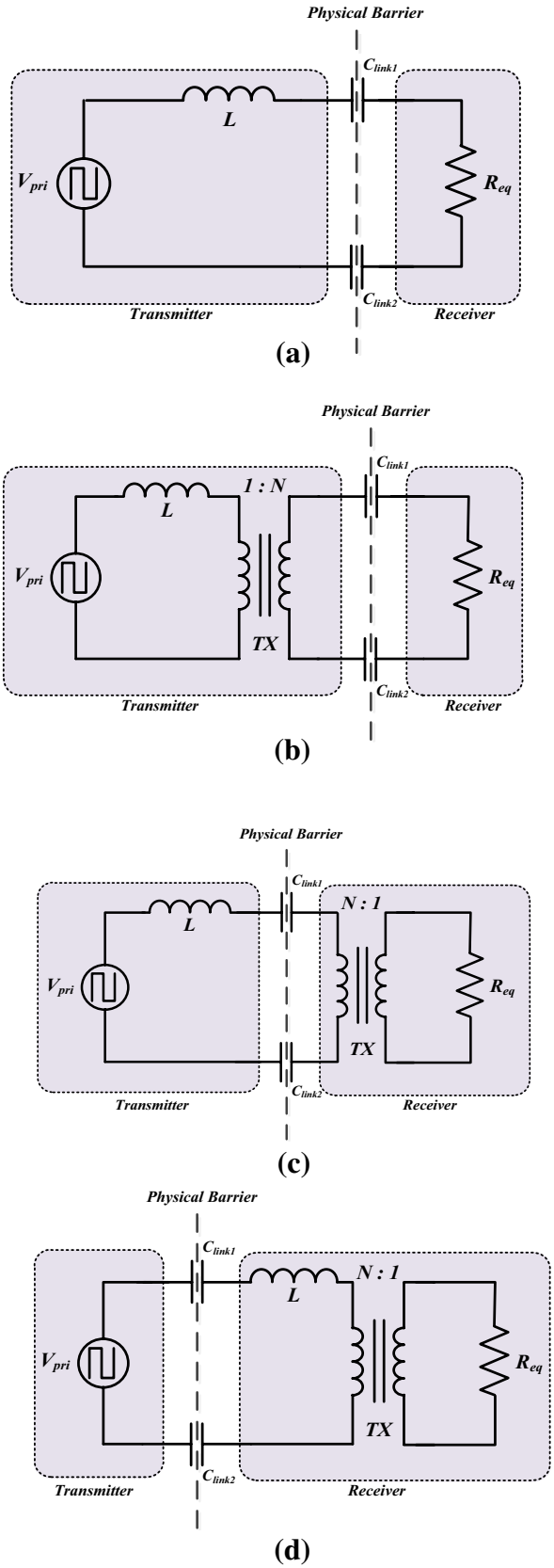


Fig. 2 Derivation of the optimum impedance matching. **a** Series inductor matching. **b** Input transformer matching with series inductor. **c** Output transformer matching with series inductor. **d** Matching scheme equivalent to **c** basic structure of C-WPT

inductor should compensate the small capacitive reactance, and the quality factor of the resonant network becomes large. The output voltage gain curve is therefore too narrow and sharp, and the voltage stress in the link capacitor increases considerably. In the input transformer matching scheme in Fig. 2b, the step-up turn ratio increases the equivalent capacitance seen from the series inductor, and thus decreases the inductance value required for the compensation. However, the matching transformer should handle the reactive power flow, and thus the total volume of the magnetic components increases.

Furthermore, since the quality factor remains the same as that in the scheme of Fig. 2a, no improvement in the voltage stress is observed. In contrast, in the case of the output transformer matching scheme shown in Fig. 2c, by the step-down turn ratio, the quality factor decreases by N^2 times, so that the voltage stress of the link capacitor is lower than that of the input transformer matching structure. Moreover, the current and the voltage applied to the matching transformer are almost in phase, so the magnetic volume is greatly reduced.

Figure 3 shows the magnetic volume comparison of the impedance compensation schemes, demonstrating that the output matching transformer scheme has the minimum total magnetic volume. For ease of comparison, the operating conditions including the link capacitance (C_{link1}, $C_{link2}=200$ pF), the output power ($P_o=5$ W [10 V/0.5 A]), and resonant frequency ($\omega_o=10$ Mrad/s) are kept the same. Notice that the series inductor in Fig. 2c is the smallest among the three schemes because the step-down transformer increases the AC equivalent resistor by N^2, which greatly reduces the current flowing through the series inductor. It is therefore concluded that the output matching scheme is the best matching location among them.

In addition, if the series inductor moves to the receiver side, the equivalent structure in Fig. 2d is obtained. When the series inductor is integrated with the output matching transformer to a single magnetic core, it is possible to implement an integrated magnetic component called a leakage-enhanced transformer (LET), where the series inductor is replaced by a leakage inductance of the LET. It is expected that such a single component matching scheme will greatly simplifies the C-WPT system.

Author's personal copy

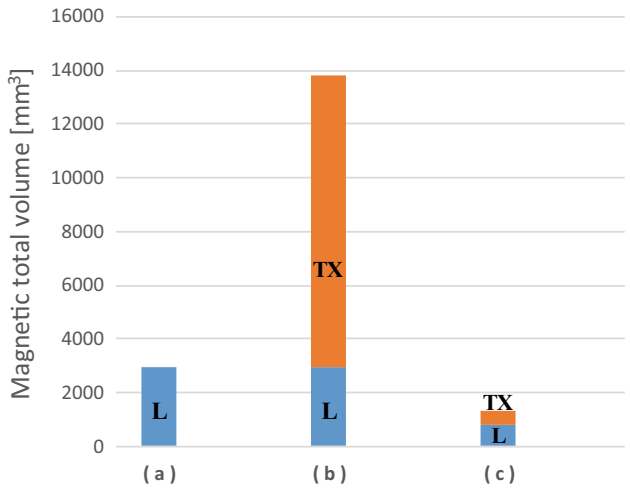


Fig. 3 Magnetic volume comparison by theoretical calculation

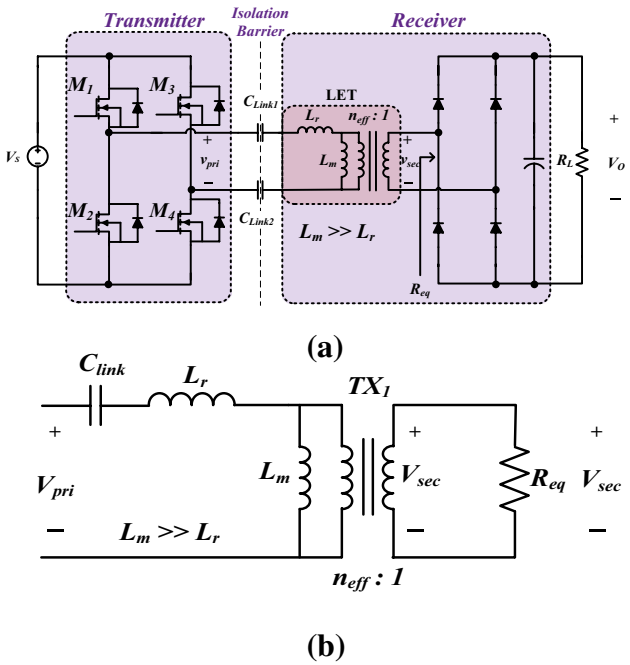


Fig. 4 Proposed LET topology. **a** Proposed topology. **b** Equivalent circuit of **a** [APR]

3 Proposed Topology Structure and LET Design

3.1 Proposed Topology Structure

Figure 4a shows the proposed topology structure. It comprises a special magnetic component called the leakage-enhanced transformer (LET) as an OMN, whereby it performs three functions simultaneously: offset the link capacitance, adjust the voltage gain, and magnify the effective load impedance. It should be noted that it is not necessary to use an additional IMN in the transmitter. Such a LET is constructed from an un-gapped core, where the leakage inductance can be controlled by the separation between the transformer windings, while the large magnetizing inductance renders the design equation simple.

Figure 4b shows the equivalent circuit with fundamental harmonic approximation (FHA) to facilitate circuit interpretation. Two link capacitors (C_{link1} and C_{link2}) are equivalently described by Clink and the LET is represented as an all primary-referenced (APR) transformer model [12]. In this transformer model, the series and parallel inductance, L_r and L_m, respectively, slightly differ from the physical leakage and magnetizing inductance. The effective turn ratio, n_{eff} of the ideal transformer block TX1 is a multiplication of the coupling coefficient and physical winding ratio.

$$n_{eff} = kN = k\frac{N_p}{N_s}. \tag{2}$$

R_{eq} is an AC equivalent resistor seen from the receiver input and is calculated from the DC load resistance.

$$R_{eq} = \frac{8}{\pi^2}R_L. \tag{3}$$

With a fundamental sine input and output voltage, V_{pri} and V_{sec}, respectively, the voltage gain formula derived from the equivalent circuit is

$$M = \frac{V_{sec}}{V_{pri}} = \frac{1/n_{eff}}{1 + Q^2\left[\left(f/f_o\right)^2 - 1\right]^2}, \tag{4}$$

where

$$f_o = \frac{1}{2\pi\sqrt{L_r C_{link}}}, \tag{5}$$

$$Q = \frac{1}{n_{eff}^2 R_{eq}}\sqrt{\frac{L_r}{C_{link}}} = \frac{1}{2\pi f_o n_{eff}^2 R_{eq} C_{link}}. \tag{6}$$

It is clearly shown that the voltage gain is maximally equal to $1/n_{eff}$, when the switching frequency, f, matches the series resonant frequency, f_o.

3.2 Leakage-Enhanced Transformer Design

The flowchart of the leakage-enhanced transformer is shown in Fig. 5 and the detailed design process is as follows. It is assumed that the output voltage V_o, input voltage V_s, the link capacitance C_{link}, and the load resistance R_L are given.

Author's personal copy

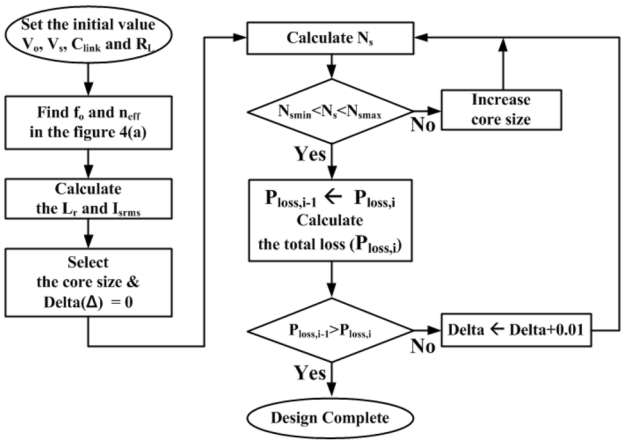


Fig. 5 Flowchart for the LET design

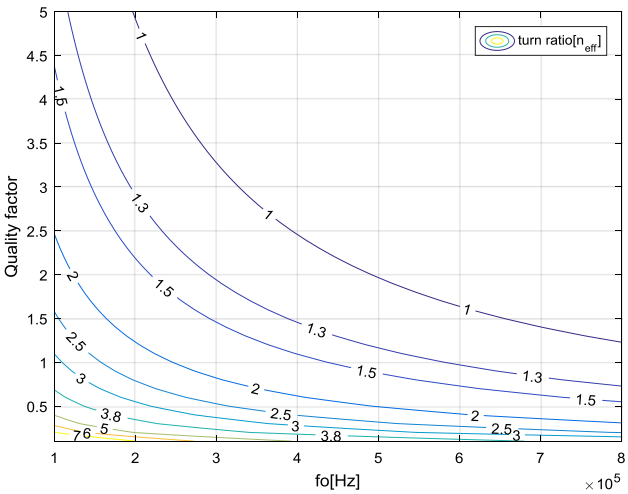


Fig. 6 Design curve

1. Effective turn ratio (n_{eff}) determination

The design curve of the LET is shown in Fig. 6, which is the result of calculating the effective turn ratio by sweeping together f_o and the quality factor (6). The resonant frequency, f_o, and the quality factor, Q, should be carefully chosen. If a higher Q value is chosen, the capacitor voltage stress ($V_{c,stress}$) increases according to (7). On the contrary, if the Q value is lower than 1, the fundamental harmonic approximation will not be validated. Meanwhile, selecting switching frequency that is too low will result in a bulky LET, whereas an excessively high switching frequency results in increased switching loss that is limited by driving circuitry and switch devices. Therefore, the appropriate resonant frequency should be selected according to the system application.

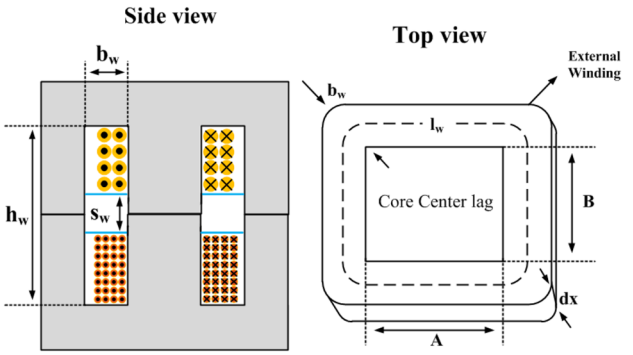


Fig. 7 LET structure in EE core

In the design curve in Fig. 6, the effective turn ratio n_{eff} is determined by f_o and Q. Subsequently, the voltage stress in the link capacitor $V_{c,stress}$, the required series inductance L_r, and the root-mean-square current I_{srms} in the transformer secondary winding are calculated using (7–9), respectively.

$$V_{c,stress} = \frac{\pi}{4} Q V_s, \tag{7}$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_{link}}, \tag{8}$$

$$I_{srms} = \frac{V_{pri}}{\sqrt{2} n_{eff} R_{eq}}. \tag{9}$$

2. Core size selection

If the switching frequency (f) is close to the resonant frequency (f_o), the transformer core can be selected using the following area product (A.P) equation.

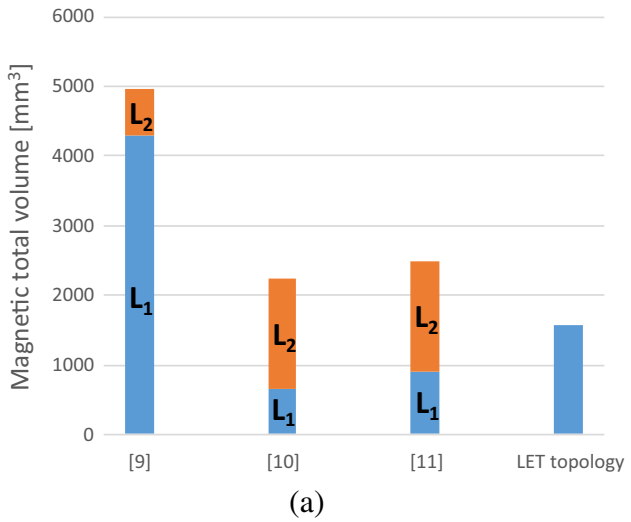
$$A_e A_w \geq \frac{10^4 P_o}{K_f B_{max} f K_u J_{rms}}, \tag{10}$$

where A_e is the core cross-sectional area, A_w is the winding area, A_{cu} is the wire cross-sectional area, and B_{max} is the maximum magnetic flux density of the core material, which can be obtained using the Steinmetz equation [13]. K_f uses the value of 4 as the waveform factor, K_u uses the value of 0.6 as the winding fill factor, and J_{rms} uses the value of 500 A/cm^2 as the maximum current density in a wire conductor [14].

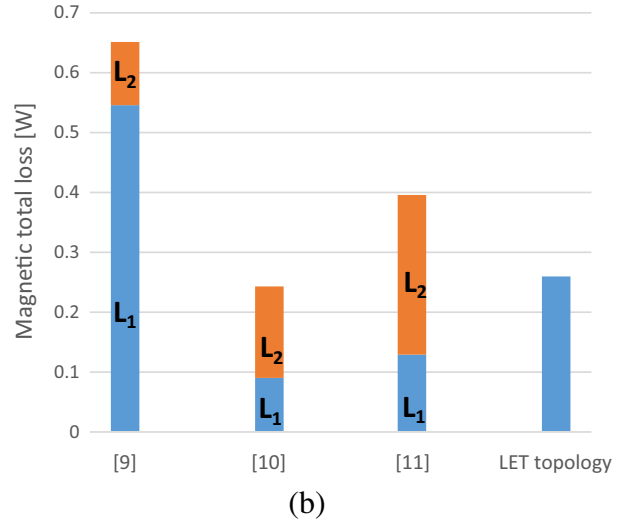
3. Number of turns and the separation between windings

First, the minimum and maximum numbers of the secondary turns are found from (11) and (12), respectively, from the core dimension data.

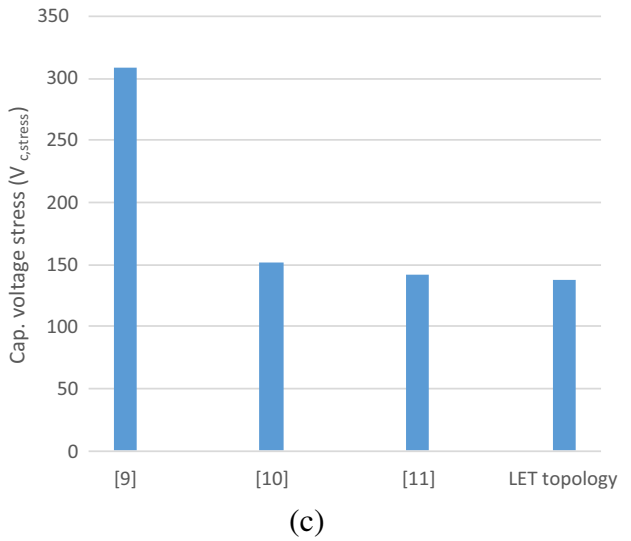
Author's personal copy



(a)



(b)



(c)

Fig. 8 Performance comparisons. **a** Volume comparison. **b** Loss comparison. **c** Link capacitor voltage stress comparison

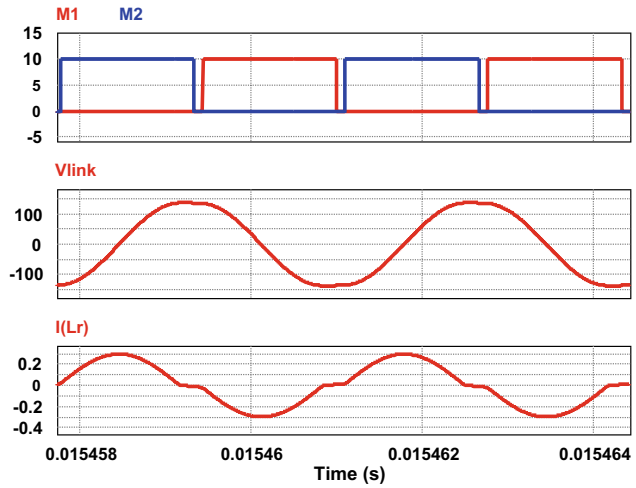


Fig. 9 Simulation waveforms

$$N_{smin} \geq \frac{V_{sec}(10^4)}{A_e B_{max} f K_f}, \tag{11}$$

$$N_{smax} \leq \frac{K_u A_w (1-\Delta)}{2A_{cu}}, \tag{12}$$

where Δ represents the separation between the two windings in Fig. 7, and is defined by the ratio of s_w to the transformer h_w as

$$\Delta = \frac{s_w}{h_w}. \tag{13}$$

Incidentally, the leakage inductance formula [12] specifies the required number of secondary turns according to Δ by (14)

$$N_s(\Delta) = \frac{k}{n_{eff}} \sqrt{\frac{L_r}{(1+k)\mu_o \frac{l_w h_w}{6 b_w}(1+2\Delta) \times 10^{-3}}}, \tag{14}$$

where h_w and b_w are the lengths of the core height and width in Fig. 7 and l_w is the average length of the winding wound on the core, which can be calculated from (15).

$$l_w = 2(A+B) + \pi b_w. \tag{15}$$

The number of turns of the transformer should be selected by the following constraint equation [15, 16].

$$N_{smin} \leq N_s(\Delta) \leq N_{smax}. \tag{16}$$

Since the maximum voltage gain is equal to $1/n_{eff}$ at resonance, the primary number of turns can be found from the effective turn ratio and the coupling coefficient using (13). For the initial calculation, it is recommended that the coupling coefficient is assumed to be a value less than 0.99.

Author's personal copy

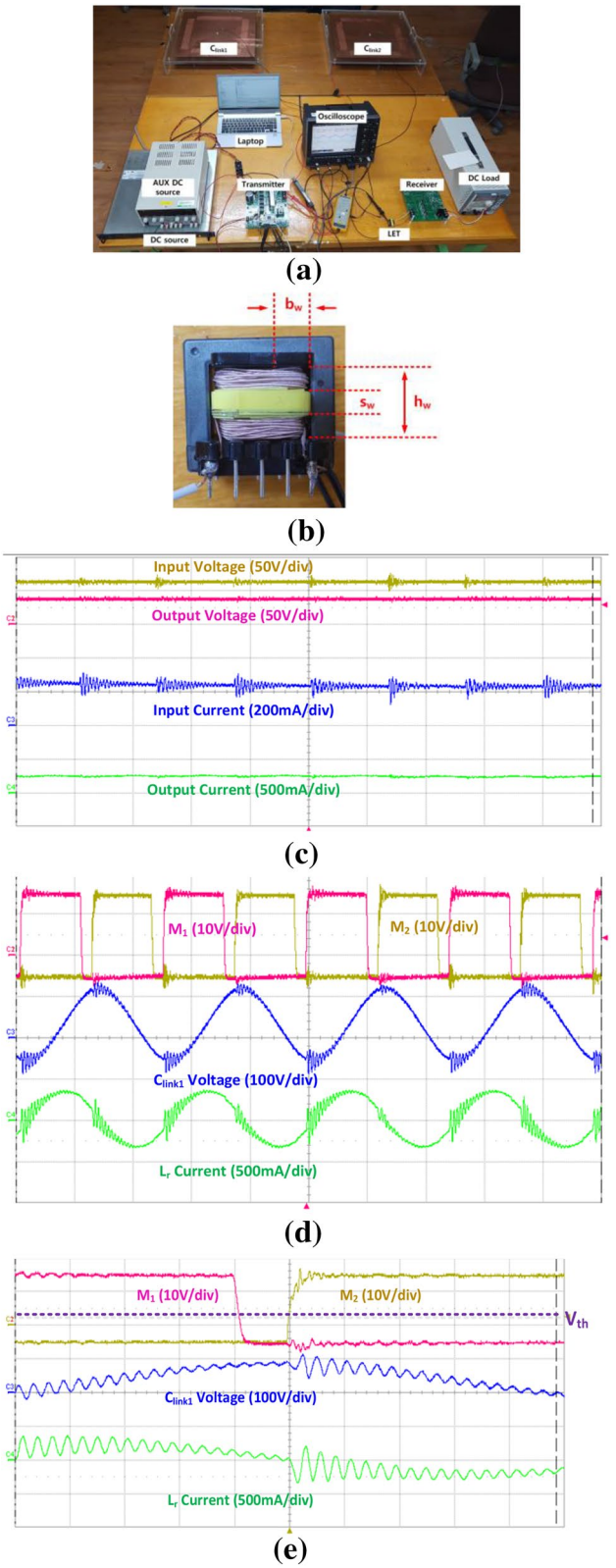


Fig. 10 Experimental results. **a** Photograph of the hardware. **b** LET. **c** Input and output voltage and current (1 μs/div). **d** Gate signals and resonant waveforms (1 μs/div). **e** Magnified view of **d** (200 ns/div)

Table 2 Design spec. and measurement results of LET

Core type	EI3026S (Samwha)
Design specification	
Effective turn ratio (n_{eff})	1.5
Num. of turns (pri.)	45
Num. of turns (sec.)	30
Winding separation (s_w)	4.39 mm
Wire size (pri. and sec.)	0.06/20 litz
Relative permeability	2400 (PL-7)
Measurement results	
Series resonant inductor (L_r)	208 μH
Parallel resonant inductor (L_m)	12.59 mH

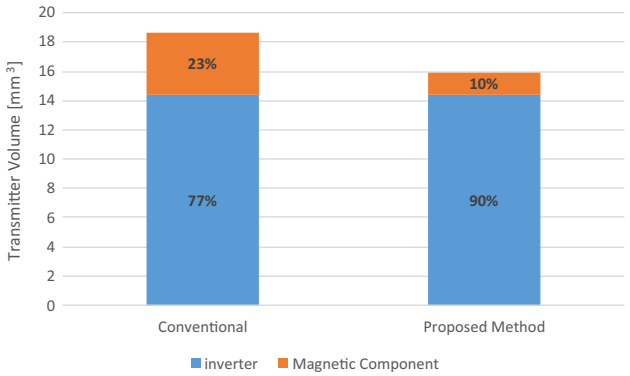


Fig. 11 Transmitter volume comparison

By adjusting Δ, the LET design can be further optimized considering the loss minimization. The Dowell curve [16] and the Steinmetz equation [13] can be used to assist the optimal Δ design process as shown in the flow chart.

4 Topology Comparison and Analysis

Based on the design procedure presented in Sect. 3, a prototype LET design was developed and the results were compared with those of another conventional matching scheme topology shown in Table 1. For fair comparison, each topology has the same operating conditions: the resonant frequency is set at 300 kHz, the input voltage is 60 V, the output is 10 W (40 V/0.25 A), and the link capacitor is 1 nF. The transmitter uses a full bridge inverter and the receiver uses a diode full-wave rectifier with an output filter, and the inductors are designed using the loss-optimization process in the literature [13–16]. Figure 8 shows the result of comparison considering the total volume and loss in the magnetic components, and the link capacitor voltage stress. It can therefore be seen that the proposed LET matching

Author's personal copy

occupies about 33% volume of the bulkiest conventional topology, dissipates only about 38% of loss of the topology with the highest loss, and generates about 44% of the link capacitor voltage stress compared with the topology that has the highest voltage stress. It should be noted that in the volume and loss analysis, the matching capacitors existing in the conventional topologies were not considered since the proposed topology does not require the capacitor components, and thus it is clear that more actual volume reduction can be achieved.

Simulation was performed to verify the proposed topology. The target output power (P_o) is 10 W, the load resistance (R_L) is 160 Ω (40 V/0.25 A), the effective link capacitor (C_{link}) connecting the transmitter and receiver is 1 nF and the input voltage (V_s) is 60 V. In the LET design process, the coupling coefficient is assumed to be 0.99. According to the design procedure in Sect. 3 with $M = 1/1.5$ ($n_{eff} = 1.5$), $f_o = 300$ kHz, and $Q = 1.46$, L_r is obtained as 281.44 μH. Based on these design parameters, the PSIM simulation waveforms are plotted in Fig. 9. The simulation was conducted assuming all switch components were ideal.

Figure 10a shows a photograph of the prototype hardware. For the full-bridge inverter and the full-wave rectifier, MOSFET (Cree, C3M0065090D) and diode (Cree, C3D16060D) were adopted, respectively. Each of the link capacitors are composed of two copper plates with 500 mm by 500 mm in the lateral dimension. The spacing between the two copper plates is 3 mm, and glass is used as the spacing material. Consequently, C_{link1} was 2.11 nF and C_{link2} was 2.01 nF. LET was constructed on a EI3026S core as shown in Fig. 10b. Table 2 shows the transformer design and measurement results of the LET, where all transformer parameters have been measured with an LCR meter (Agilent 4263B). Figure 10c shows input and output voltage and current waveform. Figure 10d shows hardware waveforms and Fig. 10e is a magnified view of Fig. 10d. In the figure, the small sub-harmonic oscillations are observed, which is caused by the resonance of the parasitic inductor in the lead wire of link capacitor and the parasitic capacitor of the LET. The resonant frequency was 379 kHz, which is slightly higher than the designed value. This is because the value of the actual resonant inductor L_r is smaller than that calculated, and the resonant frequency therefore needs to be slightly adjusted. The overall efficiency of the system is about 79% at the target power of 10 W.

Figure 11 shows a transmitter volume comparison with conventional method. The conventional method used the Ref. [9] because the topology of the proposed topology consists of the most similar form except for the transformer. The y axis of the graph indicates the transmitter volume, blue indicates the inverter, and red indicates the volume of the magnetic component. As a result, in case of using the same inverter, the proposed method has the advantage of reducing the volume of Magnetic, which occupied about 23% of the volume of the transmitter, to 10%.

5 Conclusion

This paper proposes a compact drive circuit in which no passive components are used in the transmitter side and only one magnetic component is used in the receiver side of C-WPT system. Compared to other conventional topologies, the proposed compact matching network has outstanding advantages including system simplicity, reduced circuit volume, low voltage stress, and appropriate resonant quality factor. The proposed topology is expected to be very useful for low or medium-powered wireless charging applications with restricted volume and cost requirements.

Acknowledgements This work was supported by the 2015 Research Fund of University of Ulsan, Republic of Korea.

References

1. Rim CT (2010) Technical difficulties of wireless power transfer. Trans Korean Inst Power Electron 15(6):32–39
2. Liu M, Zhao C, Song J, Ma C (2017) Battery charging profile-based parameter design of a 6.78-MHz class E2 wireless charging system. IEEE Trans Industr Electron 64(8):6169–6178
3. Patil D, Yang Z, Fahimi B (2017) A wireless powered EV battery charger for sinusoidal current charging technique with maximum efficiency control. In: 2017 IEEE Transportation Electrification Conference and Expo (ITEC), Chicago, IL, USA, pp 613–620
4. Choi SY, Gu BW, Jeong SY, Rim CT (2015) Advances in wireless power transfer systems for roadway-powered electric vehicles. IEEE J Emerg Sel Top Power Electron 3(1):18–36
5. Miller JM, Onar OC, Chinthavali M (2015) Primary-side power flow control of wireless power transfer for electric vehicle charging. IEEE J Emerg Sel Top Power Electron 3(1):147–162
6. Kline M, Izyumin I, Boser B, Sanders S (2011) Capacitive power transfer for contactless charging. In: 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, pp 1398–1404
7. Theodoridis MP (2012) Effective capacitive power transfer. IEEE Trans Power Electron 27(12):4906–4913
8. Lu F, Zhang H, Hofmann H, Mi C (2015) A double-sided LCLC-compensated capacitive power transfer system for electric vehicle charging. IEEE Trans Power Electron 30(11):6011–6014
9. You YS, Moon HW, Yi KH (2016) High frequency (MHz) LLC resonant converter for a capacitor coupling wireless power transfer (CCWPT). Trans Korean Inst Power Electron 21(2):111–116
10. Lu F, Zhang H, Hofmann H, Mi C (2018) A double-sided LC compensation circuit for loosely-coupled capacitive power transfer. IEEE Trans Power Electron 33(2):1633–1643
11. Luo B, Mai R, Chen Y, Zhang Y, He Z (2017) A voltage stress optimization method of capacitive power transfer charging system. In: 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, pp 1456–1461

Author's personal copy

12. Simone D, Adragna C, Spini C (2008) Design guideline for magnetic integration in LLC resonant converters. In: International Symposium on Power Electronics, pp 950–957
13. Erickson RW, Maksimovic D (2001) Fundamentals of Power Electronics, 2nd edn, chap 13. Kluwer Academic Press
14. Mclyman CWT (2011) Transformer and inductor design handbook, 4th edn. CRC Press, Boca Raton
15. Snelling EC (1969) Soft ferrites-properties and applications, 2nd edn. Iliffe Books LTD, London, pp 337–358
16. Wojda RP, Kazimierczuk MK (2012) Winding resistance of litz-wire and multi-strand inductors. IET Power Electron 5(2):257–268

Hee-Su Choi received the B.S. and M.S. degrees in electrical engineering from Ulsan University, Ulsan, in 2016 and 2018, respectively. In 2018, he joined the Silicon Mitus, Inc., Pangyo, Seoul, Korea, where he is currently an Associate Engineer with the System and Application Engineering. His current research interests include wireless power transfer system, magnetics and PMIC application system.

Sung-Jin Choi received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, in 1996, 1998, and 2006, respectively. From 2006 to 2008, he was a Research Engineer with Palabs Company, Ltd., Seoul. From 2008 to 2011, he was with Samsung Electronics Company, Ltd., Suwon, Korea, as a Principal Research Engineer, developing LED drive circuits and wireless battery charging system. In 2011, he joined the University of Ulsan, Ulsan, Korea, where he is currently an Associate Professor with the School of Electrical Engineering. In 2018, he was with San Diego State University, San Diego, CA, USA, as a Visiting Scholar. His current research interests include component modeling, topology and control of high-frequency switching converters, and power electronics for renewable energy sources.